

John A. Z.

- [illegible]

Sub
a2

the step of performing the first plurality of intermediate butterfly computations of the first 1D IDCT and the second 1D IDCT including performing a second plurality of intermediate butterfly computations simultaneously in parallel.

5 6. The method for performing the IDCT on the plurality of input coefficients as
 claimed in claim 4, wherein:

the step of performing the intermediate butterfly computation of the first 1D IDCT and the second 1D IDCT including performing each intermediate butterfly computation in a single instruction.

10 7. The method for performing the IDCT on the plurality of input coefficients as
claimed in claim 3, wherein:

the step of maintaining the initial product at no more than 16-bits including rounding the initial product utilizing a round near positive (RNP) rounding scheme.

8. The method for performing the IDCT on the plurality of input coefficients as
15 claimed in claim 1, wherein:

performing the first and second 1D IDCT including rounding utilizing a RNP rounding scheme and not utilizing a rounding away from zero (RAZ) rounding scheme.

9. The method for performing the IDCT on the plurality of input coefficients as
20 claimed in claim 8, wherein:

the step of rounding and shifting including rounding utilizing a RAZ rounding scheme.

10. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

25 the step of performing the intermediate butterfly computation of the first 1D
IDCT and the second 1D IDCT including performing each intermediate butterfly
computation in a single instruction.

11. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 10, wherein:

the step of performing the first plurality of intermediate butterfly computations of the first 1D IDCT and the second 1D IDCT including performing a second plurality of intermediate butterfly computations simultaneously in parallel.

12. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of performing the first plurality of intermediate butterfly computations including performing each intermediate butterfly computation in a single instruction.

13. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 12, wherein:

the step of performing the first plurality of intermediate butterfly computations including performing a second plurality of intermediate butterfly computations simultaneously in parallel.

14. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 13, wherein:

the step of performing a second plurality of intermediate butterfly computations simultaneously in parallel including performing at least four intermediate butterfly computations simultaneously in parallel.

15. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of shifting the input coefficients left a plurality of bits including shifting the input coefficients left at least 4-bits.

16. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, further comprising:

loading the input coefficients into at least one register including loading a plurality of the input coefficients simultaneously in parallel and shifting the input coefficients left a plurality of bits prior to the step of performing the first 1D IDCT.

17. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 16, wherein:

the step of loading a plurality of coefficients simultaneously in parallel including loading at least four coefficients simultaneously in parallel.

18. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of shifting the input coefficients left including shifting a plurality of the input coefficients left simultaneously in parallel.

19. The method for performing the IDCT on the plurality of input coefficients as

July 12
claimed in claim 18, wherein:

the step of shifting a plurality of the coefficients left simultaneously including shifting at least four coefficients simultaneously in parallel.

- 5 20. A method for performing an inverse discrete cosine transform (IDCT) on a plurality of input coefficients, the method for performing the IDCT comprising:
- performing a first one directional (1D) IDCT resulting in a plurality of first 1D IDCT coefficients including utilizing a round-near-positive (RNP) rounding scheme;
- 10 performing a second 1D IDCT resulting in a plurality of second 1D IDCT coefficients including utilizing a round-near-positive (RNP) rounding scheme; and
- rounding and shifting the plurality of second 1D IDCT coefficients resulting in a plurality of output coefficients including rounding utilizing a round away from zero (RAZ) rounding scheme.
- 15 21. The method for performing the IDCT as claimed in claim 20, wherein:
- the step of rounding and shifting including rounding utilizing the RAZ rounding scheme including:
- shifting the second 1D IDCT final coefficient right a plurality of bits resulting in a shifted final coefficient;
- adding a conditional constant with the shifted final coefficient resulting
- 20 in a conditional product;
- adding the second 1D IDCT final coefficient with the conditional product resulting in a compensated final product; and
- shifting the compensated final product right a plurality of bits.
22. The method for performing the IDCT as claimed in claim 21, wherein:
- 25 the step of shifting the second 1D IDCT final coefficient including shifting the second 1D IDCT final coefficient right at least 15-bits.
23. The method for performing the IDCT as claimed in claim 21, wherein:
- the step of adding the conditional constant including:
- adding 32 if the second 1D IDCT final coefficient is positive; and
- 30 adding 31 if the second 1D IDCT final coefficient is negative.
24. The method for performing the IDCT as claimed in claim 21, wherein:
- the step of shifting the compensated final product left including shifting the

Subi
az

- [illegible]

THE 2015

32. The method for decompressing compressed data as claimed in claim 31, wherein:

the IDCT is performed in less than 397 cycles.

33. The method for decompressing compressed data as claimed in claim 32, wherein:

complying with an Institute of Electrical and Electronics Engineers (IEEE)
1180 accuracy standard.

34. The method for decompressing compressed data as claimed in claim 33, wherein:

10 implementing the IDCT utilizing single instruction multiple data instructions
(SIMD).

35. The method for decompressing compressed data as claimed in claim 34, wherein:

performing at least four SIMD instructions simultaneously in parallel.

15 36. The method for decompressing compressed data as claimed in claim 31,
wherein:

performing the first 1D IDCT and the second 1D IDCT such that four coefficients are operated on simultaneously in parallel.

20 37. An apparatus for decompressing a compressed data signal, comprising:
a means for loading a plurality of input coefficients into at least one register;
a means for shifting the input coefficients a plurality of bits coupled with the
register configured to receive the input coefficients and produce shifted input
coefficients;

25 a means for performing a first one directional (1D) Inverse Discrete Cosine Transform (IDCT) coupled with the means for shifting the input coefficients configured to receive the shifted coefficients and produce a first 1D IDCT output matrix;

30 a means for performing the first IDCT configured to transpose the first 1D IDCT output matrix and to produce a first transposed IDCT output matrix;

a means for performing a second 1D IDCT on the transposed IDCT output

Sub
a2

Transform (IDCT) including utilizing a round near positive (RNP) rounding scheme producing a first IDCT output matrix;

transposing the first IDCT output matrix producing a transposed IDCT output matrix;

5 performing a second 1D IDCT on the transposed IDCT output matrix including utilizing a RNP rounding scheme producing a second IDCT output matrix including a plurality of components;

rounding away from zero and shifting each of the components of the second IDCT output matrix producing a rounded IDCT output matrix; and

10 transposing the rounded IDCT output matrix producing a decompressed output.

Add
a2

001427 1001427